Nonvolatile Semiconductor Memory Technology

A Comprehensive Guide to Understanding and Using NVSM Devices

Edited by

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defined as the "0" or erased state and the "1" or written (programmed) state, as illustrated in Fig. 1.4.

From the basic theory of the MOS transistor, the threshold voltage is given by

$$V_{TH} = 2\phi_F + \phi_{ms} - \frac{Q_I}{C_I} - \frac{Q_D}{C_I} - \frac{Q_T}{\epsilon_I} d_I \tag{1.1}$$

where ϕ_{MS} = the work function difference between the gate and the bulk material
ϕ_F = the Fermipotential of the semiconductor at the surface
Q_I = the fixed charge at the silicon/insulator interface
Q_D = the charge in the silicon depletion layer
Q_T = the charge stored in the gate insulator at a distance d_I from the gate
C_I = the capacitance of the insulator layer
ϵ_I = the dielectric constant of the insulator

Thus, the threshold voltage shift, caused by the storage of the charge Q_T is given by

$$\Delta V_{TH} = -\frac{Q_T}{\epsilon_I} d_I \tag{1.2}$$

The information content of the device is detected by applying a gate voltage V_{read} with a value between the two possible threshold voltages. In one state, the transistor is conducting current, while, in the other, the transistor is cut off. When the power supply is interrupted, the charge should, of course, remain stored in the gate insulator in order to provide a nonvolatile device.

The storage of charges in the gate insulator of a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes.

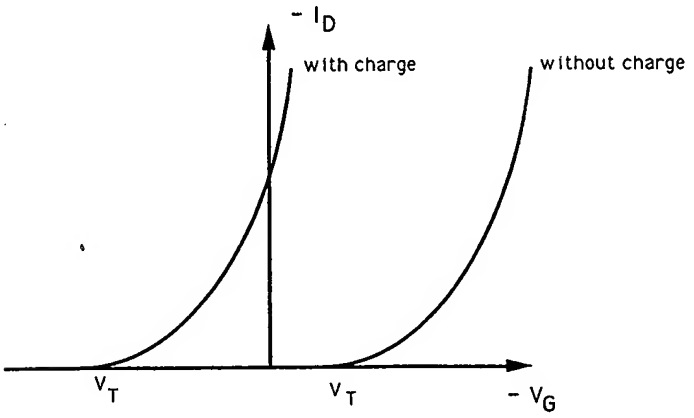

Figure 1.4 Influence of charge in the gate dielectric on the threshold of a p-channel transistor.

The first class of devices is based on the storage of charge on a conducting or semiconducting layer that is completely surrounded by a dielectric, usually thermal oxide, as shown on Fig. 1.5*a*. Since this layer acts as a completely electrically isolated gate, this type of device is commonly referred to as a floating gate device [1.6, 1.7].

In the second class of devices, the charge is stored in discrete trapping centers of an appropriate dielectric layer. These devices are, therefore, usually referred to as charge-trapping devices. The most successful device in this category is the MNOS device (metal–nitride–oxide–semiconductor) structure [1.2, 1.8], in which the insulator consists of a silicon nitride layer on top of a very thin silicon oxide layer, as shown in Fig. 1.5*b*. Other possibilities, such as Al_2O_3 (MAOS) and Ta_2O_5 (MTOS) [1.9, 1.10], have never been successfully exploited.

Further details on the cell types, features, and new developments, as well as a comparison of these classes of nonvolatile memory cells, are given in Section 1.4.

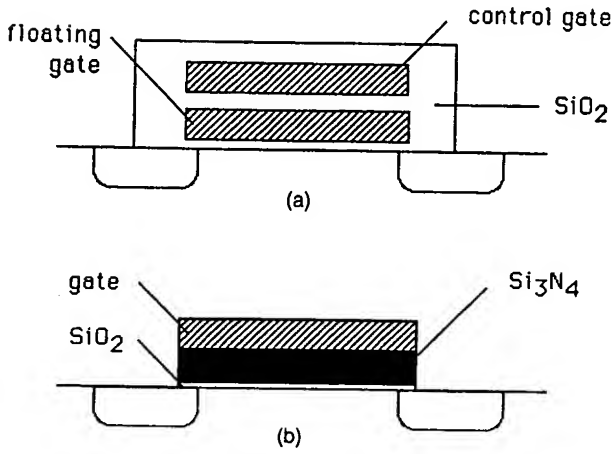

Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (*a*) floating gate devices; (*b*) charge-trapping devices (MNOS device).

1.1.2 Short Historical Review

The idea of using a floating gate device to obtain a nonvolatile memory device was suggested for the first time in 1967 by D. Kahng and S. M. Sze [1.1]. This was also the first time that the possibility of nonvolatile MOS memory devices was recognized.

The memory transistor that they proposed started from a basic MOS structure, where the gate structure is replaced by a layered structure of a thin oxide I_1, a floating but conducting metal layer M_1, a thick oxide I_2, and an external metal gate M_2, as shown in Fig. 1.6. This device is referred to as the MIMIS (metal–insulator–metal–insulator–semiconductor) cell. The first dielectric I_1 has to be extremely thin in order to obtain a sufficiently high electric field to allow tunneling of electrons toward the floating gate. These electrons are then "captured" in the conduction band of the floating gate M_1, if the dielectric I_2 is thick enough to prevent discharging. When the gate voltage is removed, the field in I_1 is too small to allow